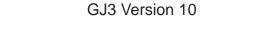
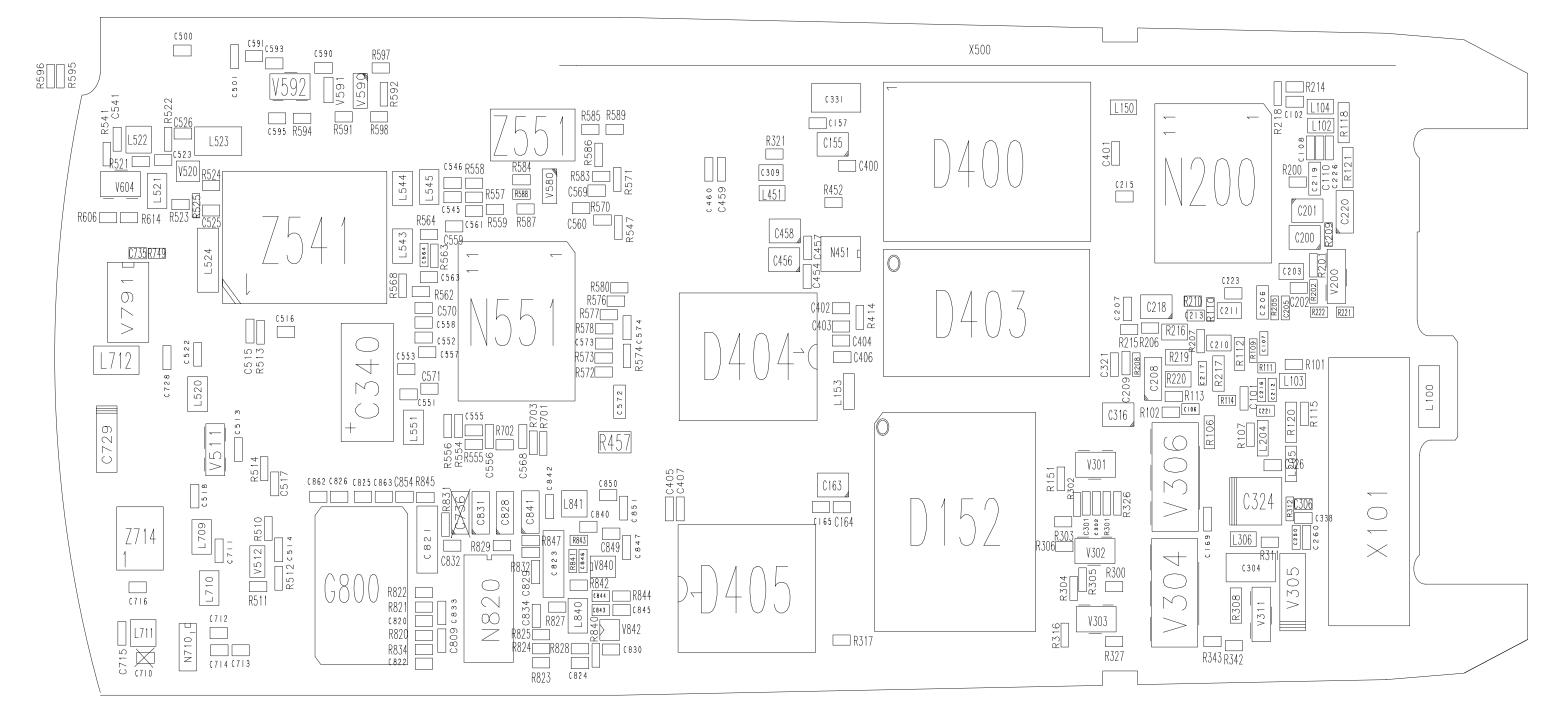
Figure 24 Component Layout Top







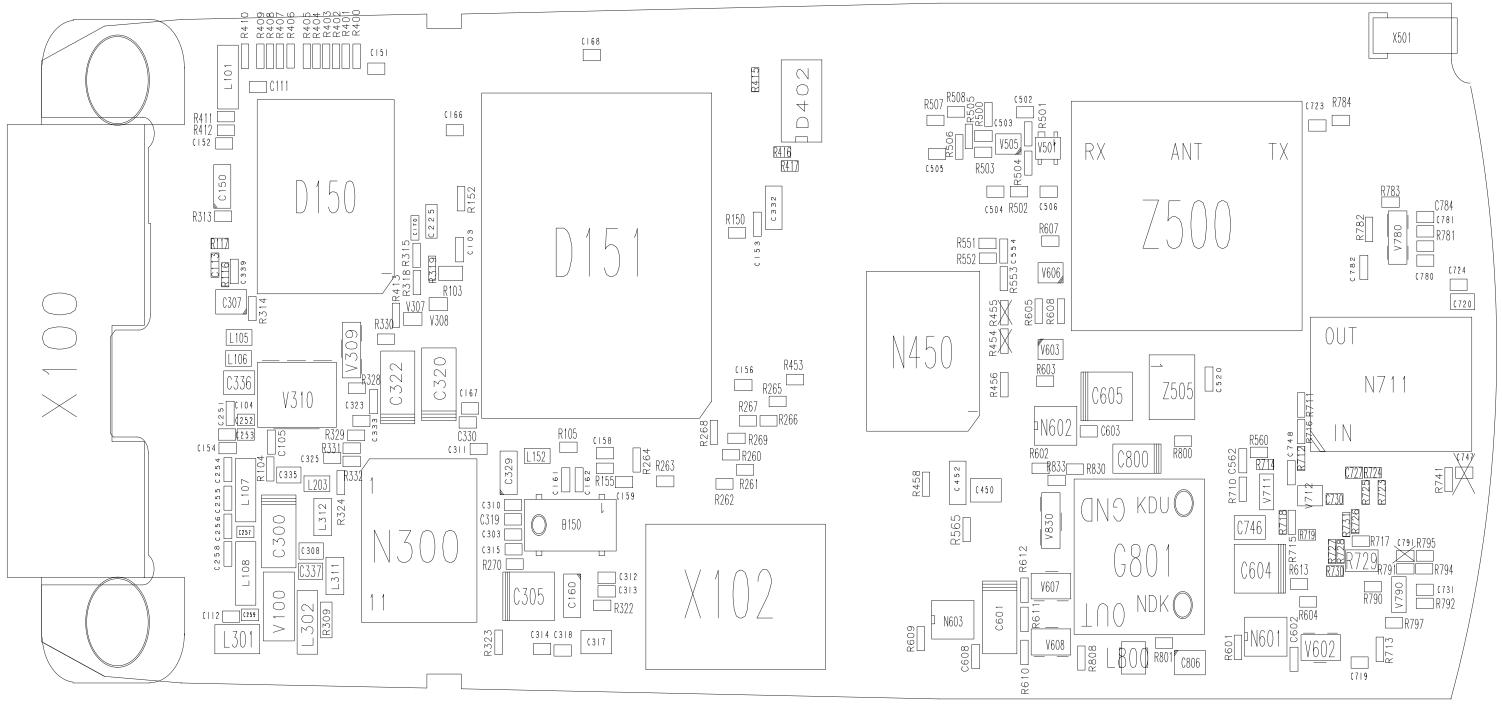


Figure 26 System Block Diagram

Figure 26 System Block Dia	gram	RFC RXI
		RXQ
S	YS	
RXQ RXI		AFC
RFC	AFC TXC TXQP	TXC TXQP
	TXQN TXIP	TXQN TXIP TXIN
	TXIN SCLK	SCLK
	SDATA SENA1	SDATA SENA1 RXPWR
	R X P WR T X P WR T X P	TXPWR TXPWR TXP
	SYNTHPWR	SYNTHPWR
	RFOUT	
	PDATA0	PDATAO
	VXOENA VBATT	VBATT ▲
	VREF_2.5V RFO_CONT	VXOENA
	RFCGND	VREF_2.5V

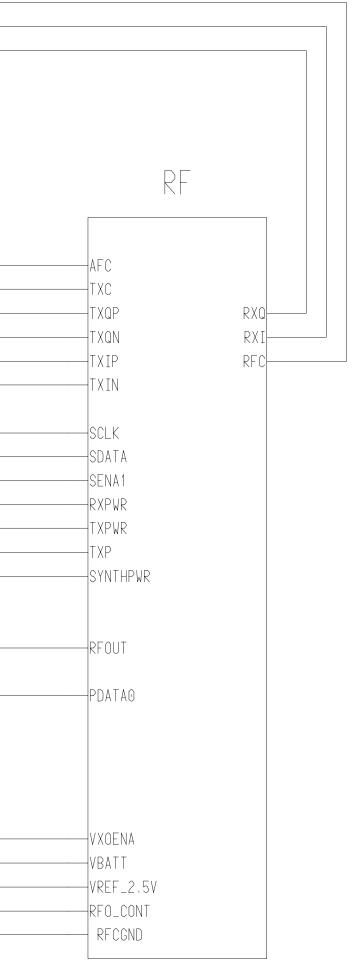
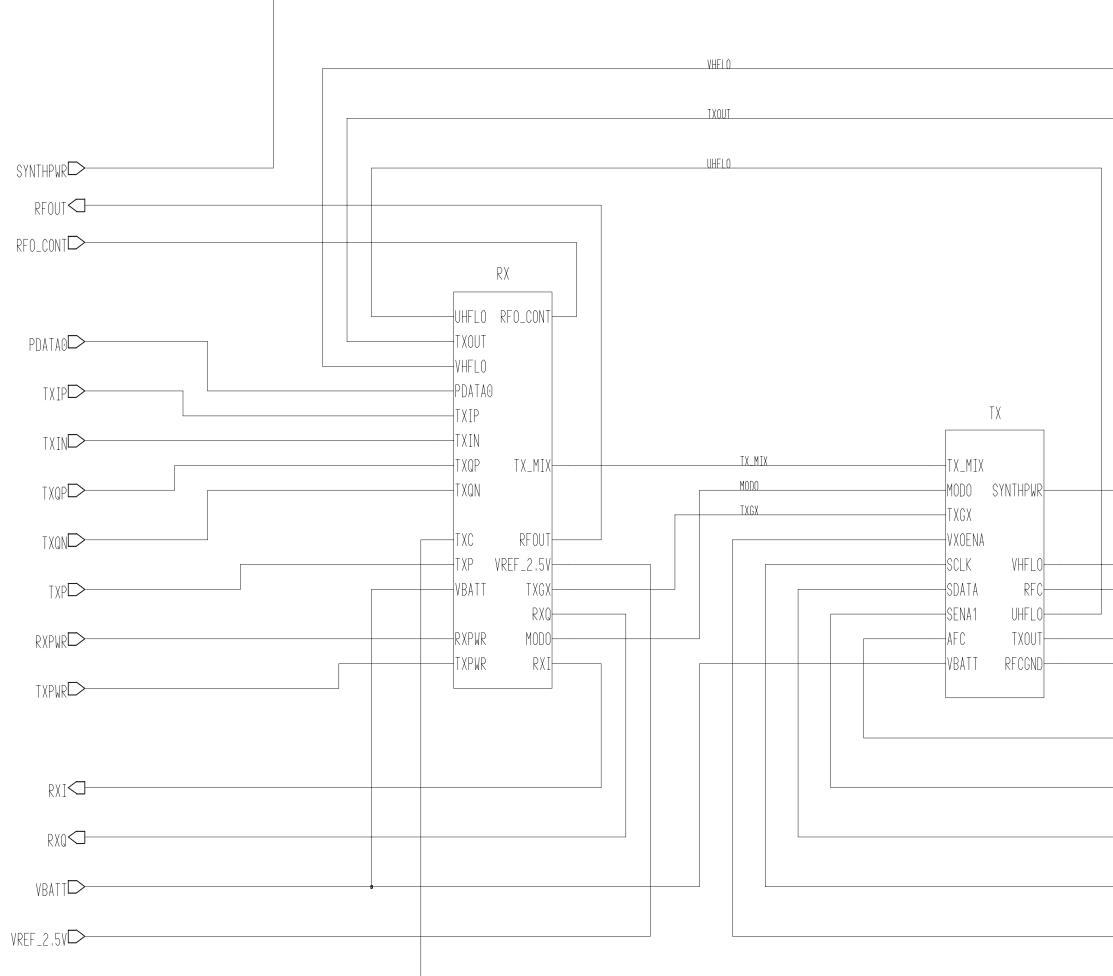
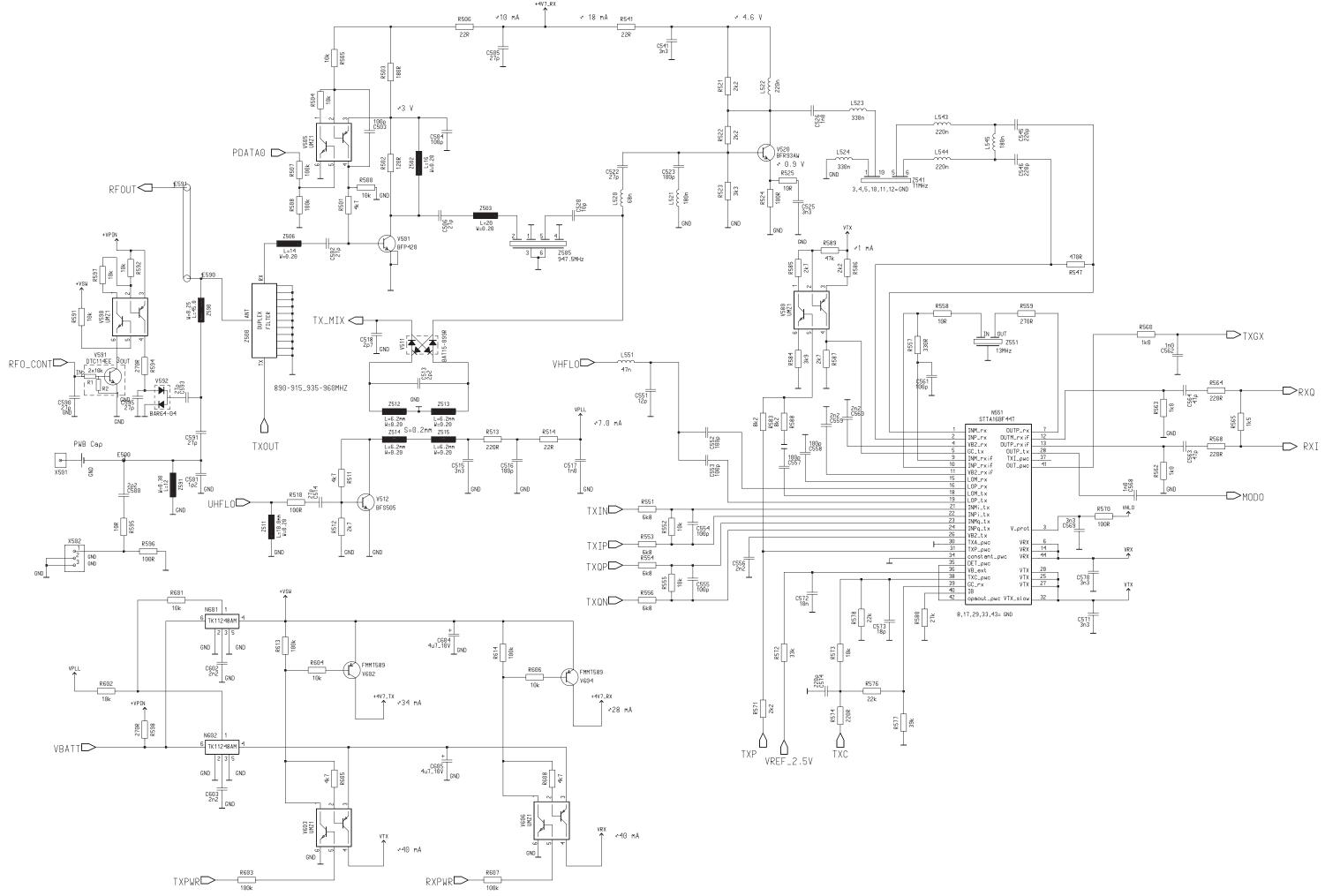


Figure 27 RX/TX Block Diagram



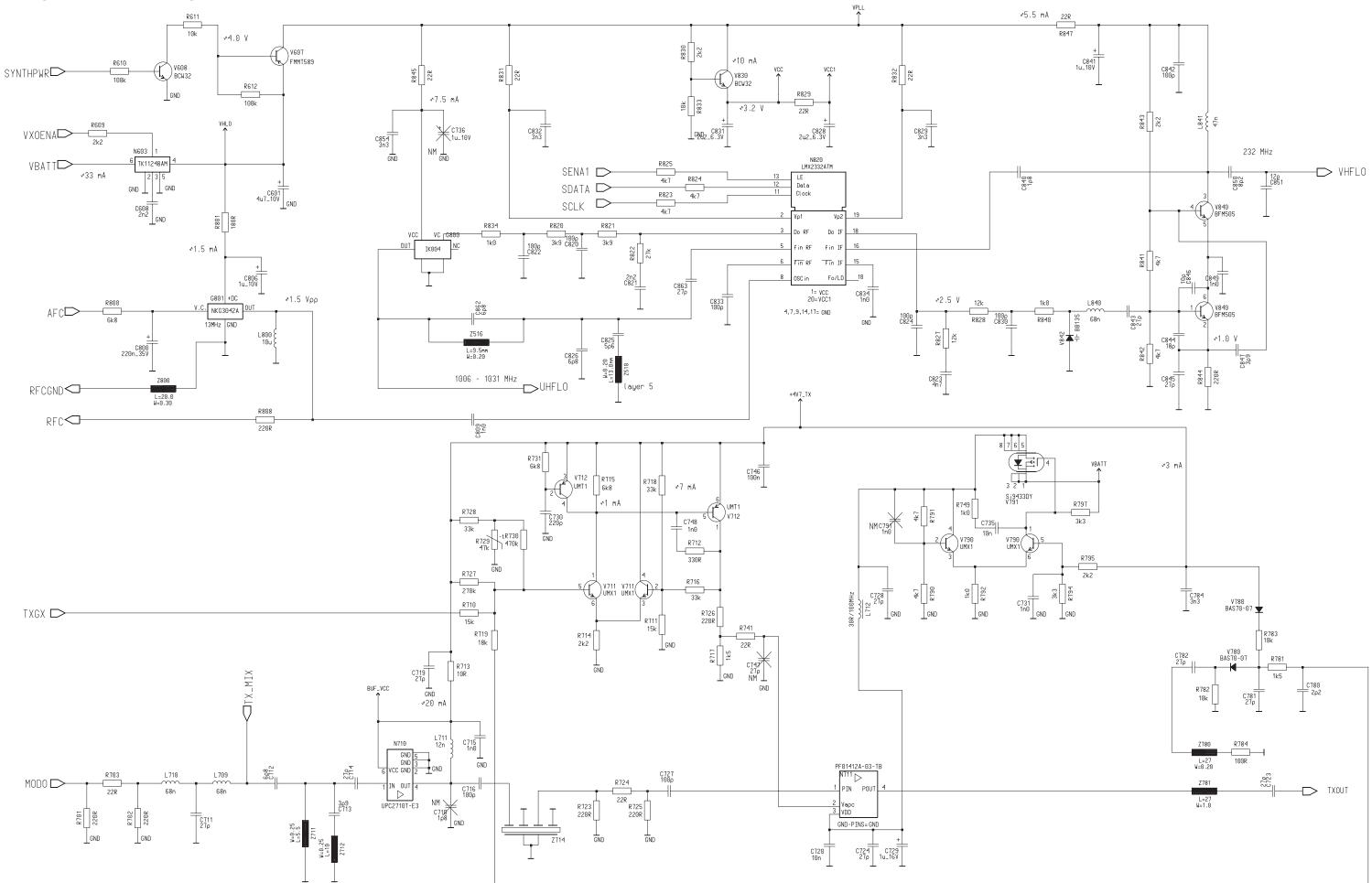
NHE 8/9
RFCGND
SENA1
SDATA
SCLK

Figure 28 RX Circuit Diagram



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Figure 29 TX Circuit Diagram



NM = NOT MOUNTED

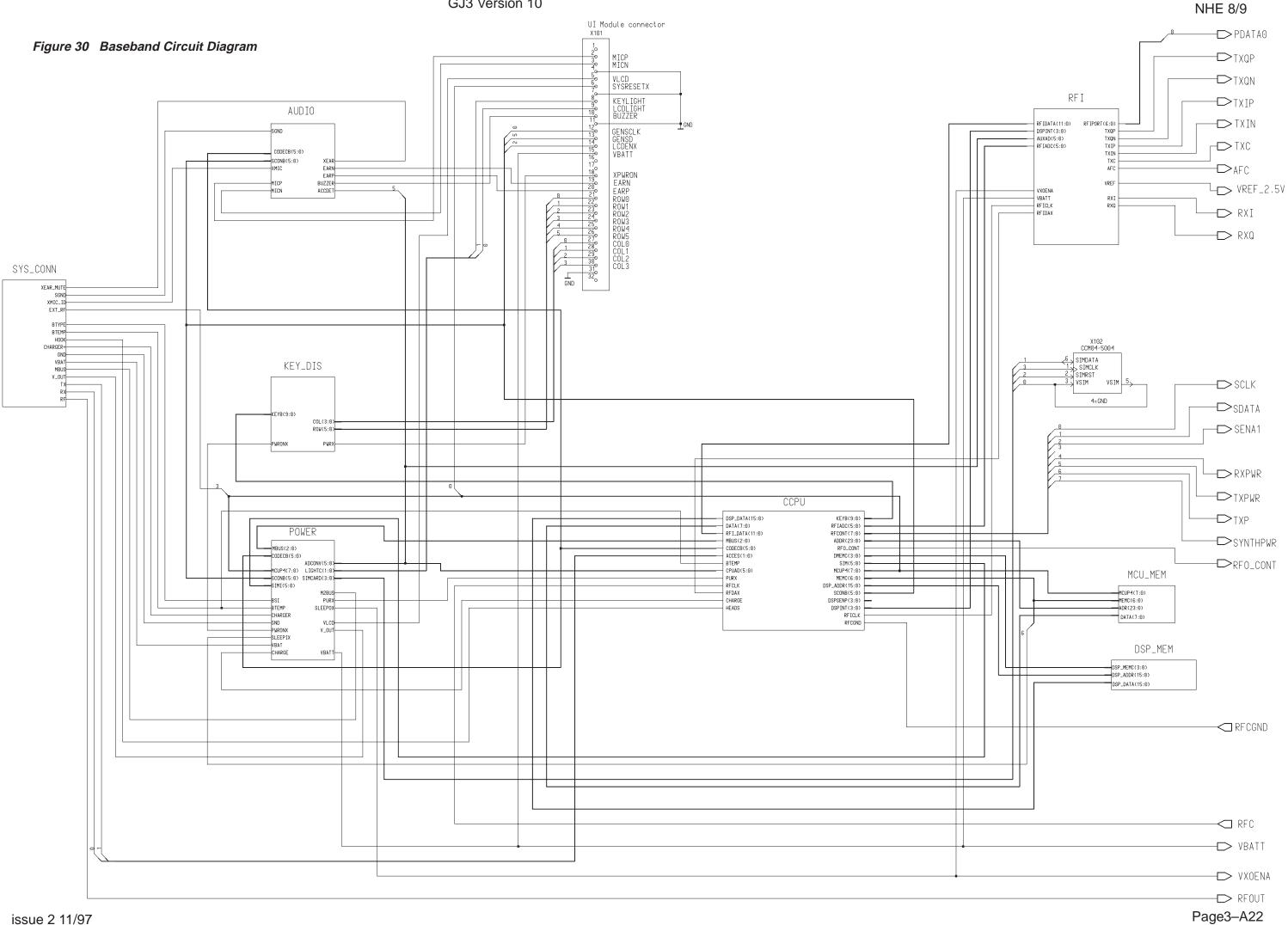
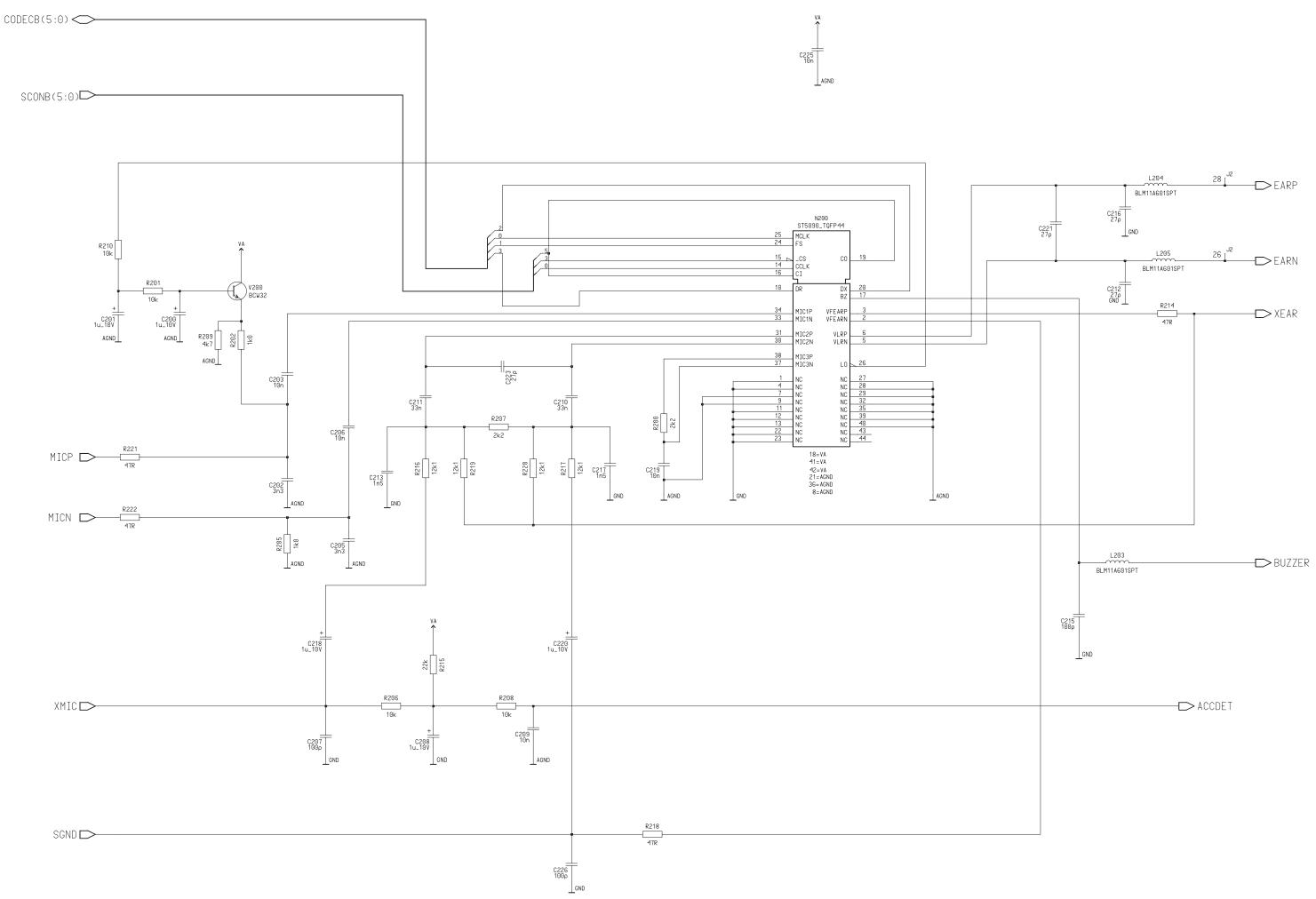


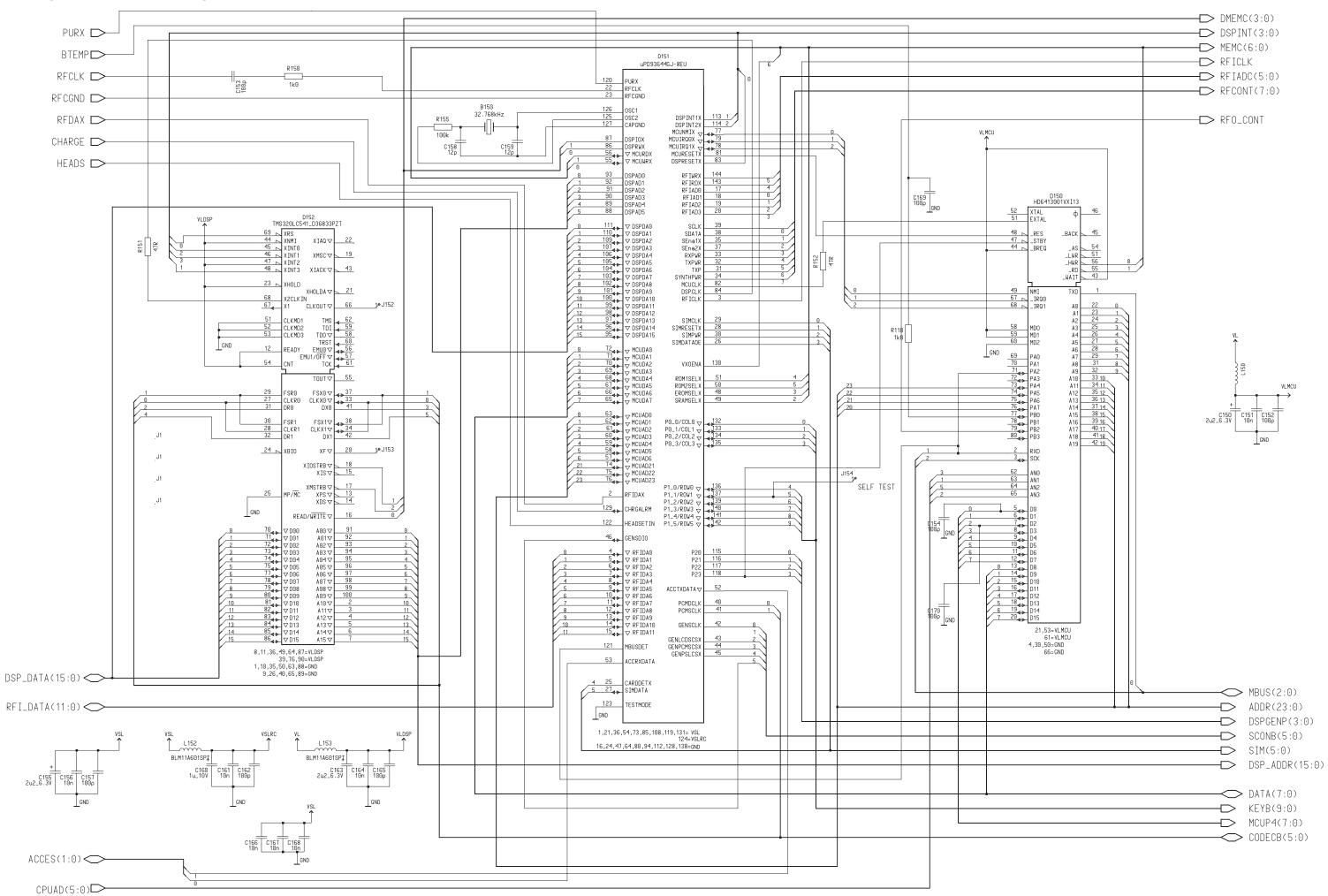


Figure 31 Audio Circuit Diagram



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Figure 32 CPU Circuit Diagram



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NHE 8/9

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Figure 33 DSP Circuit Diagram

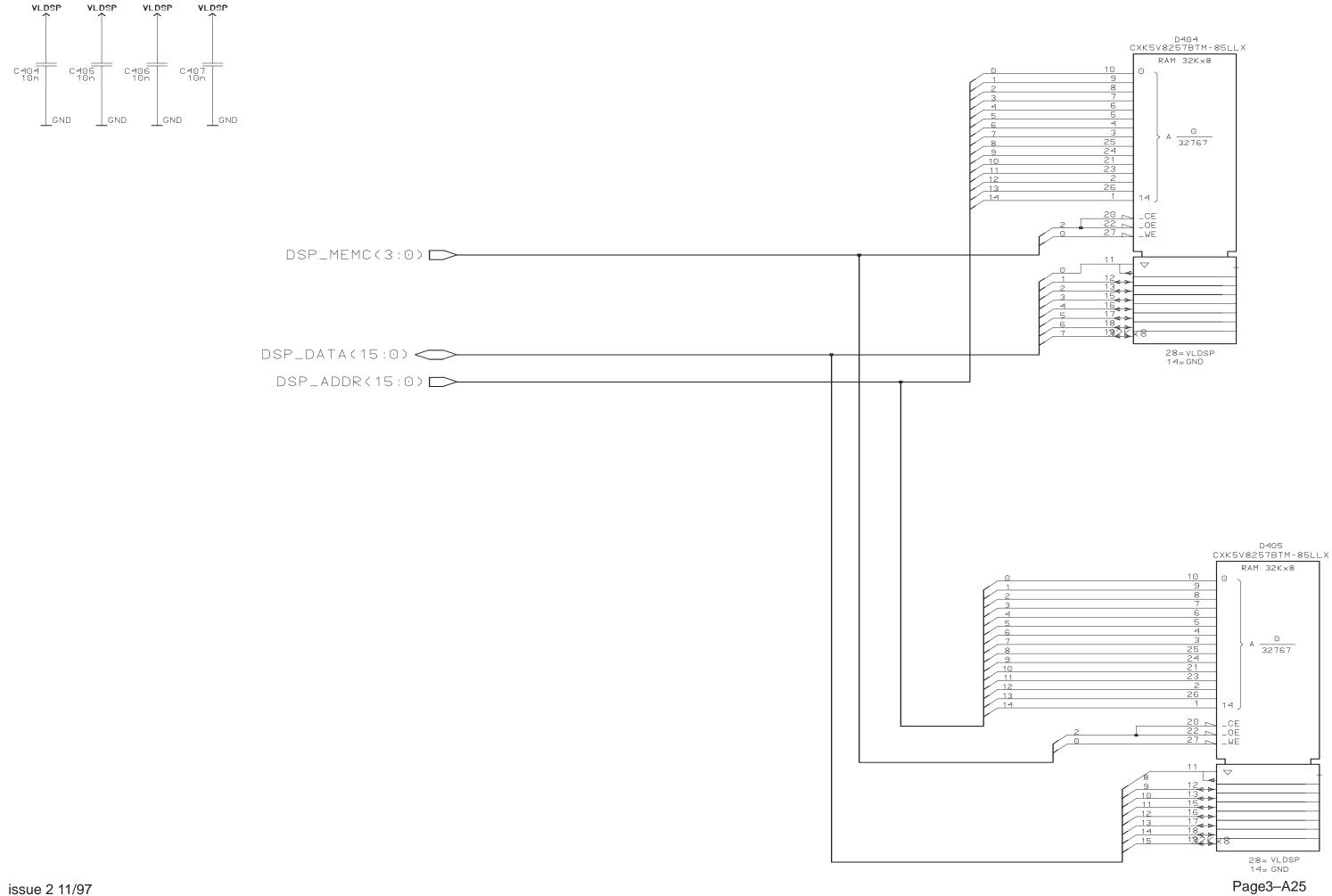
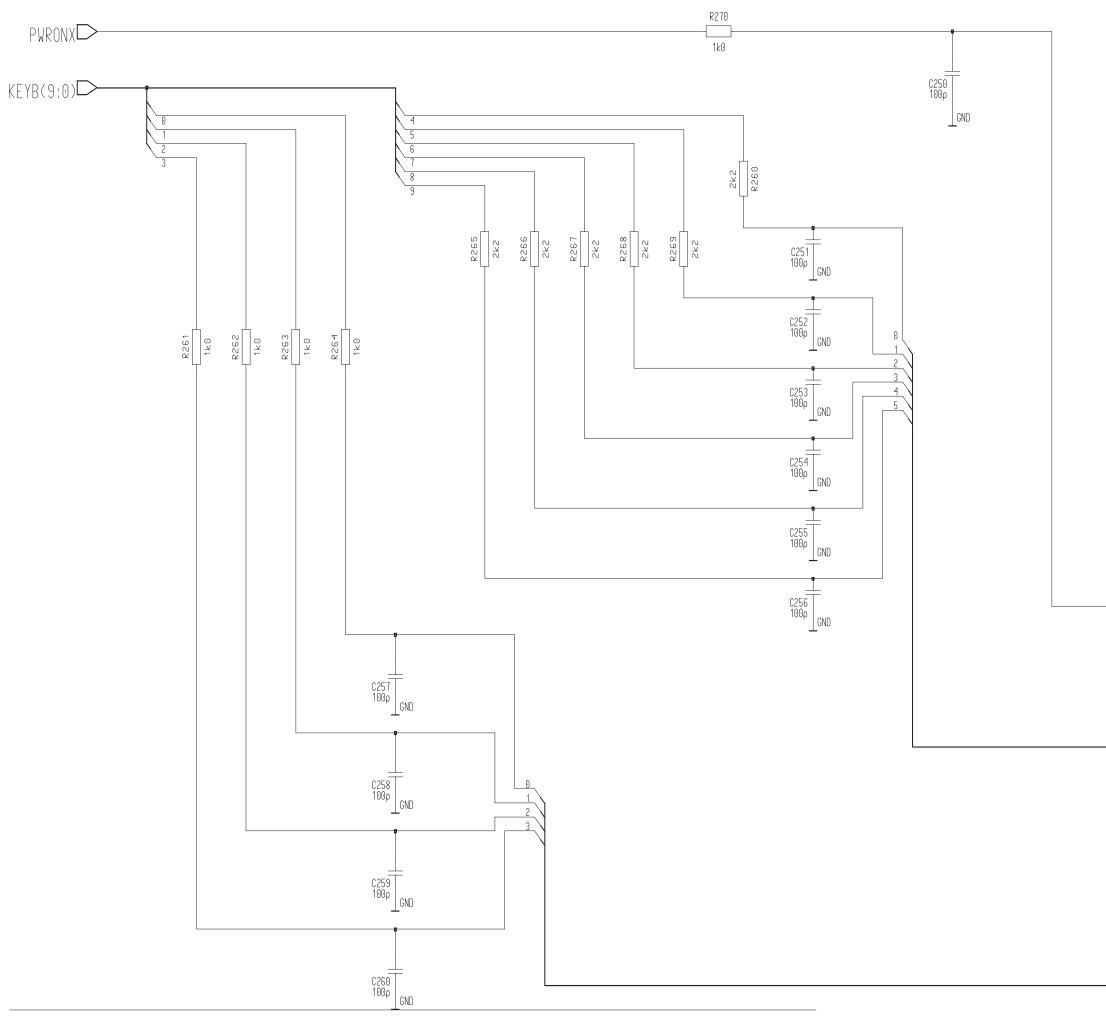




Figure 34 Keyboard / Display Interface

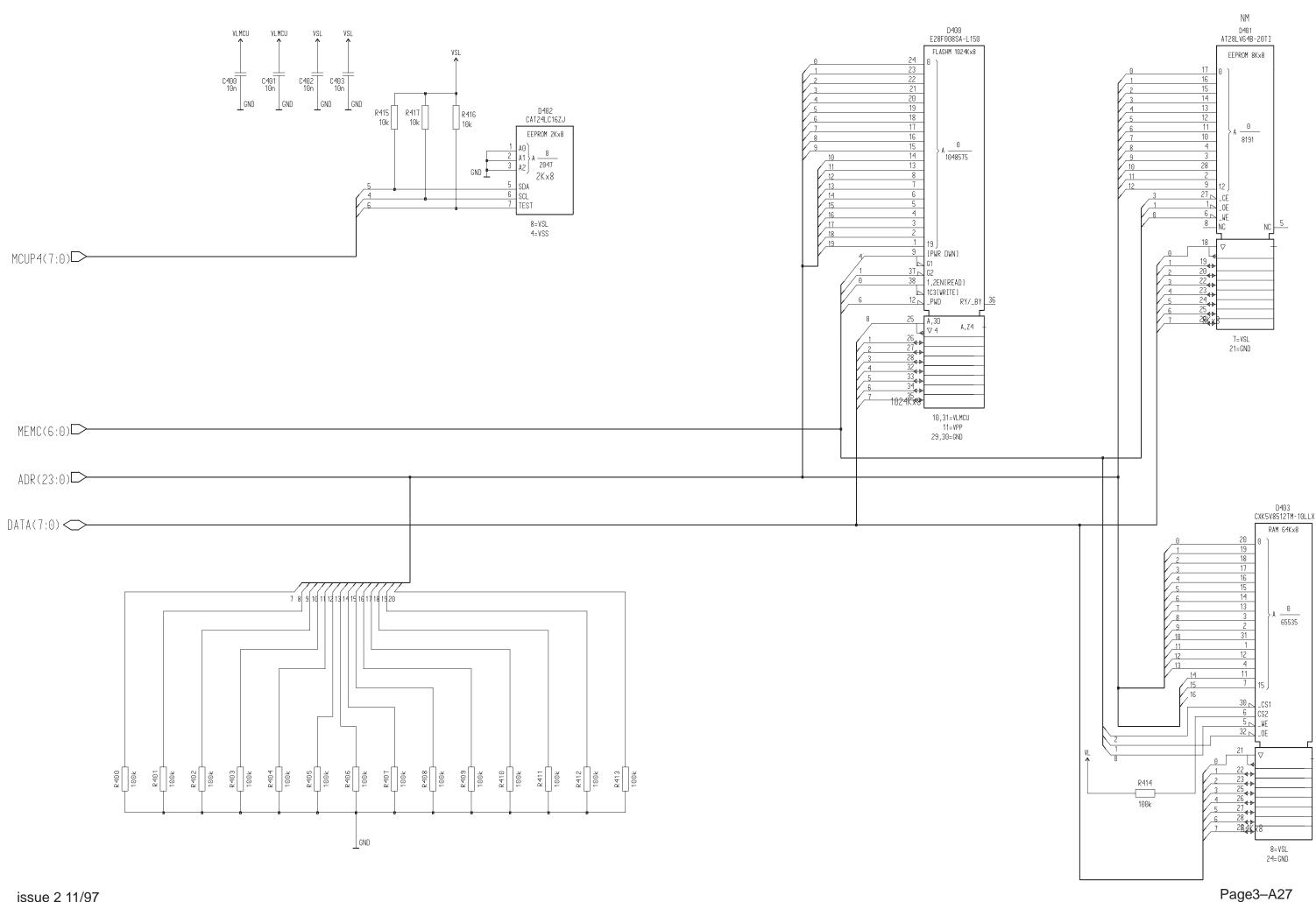


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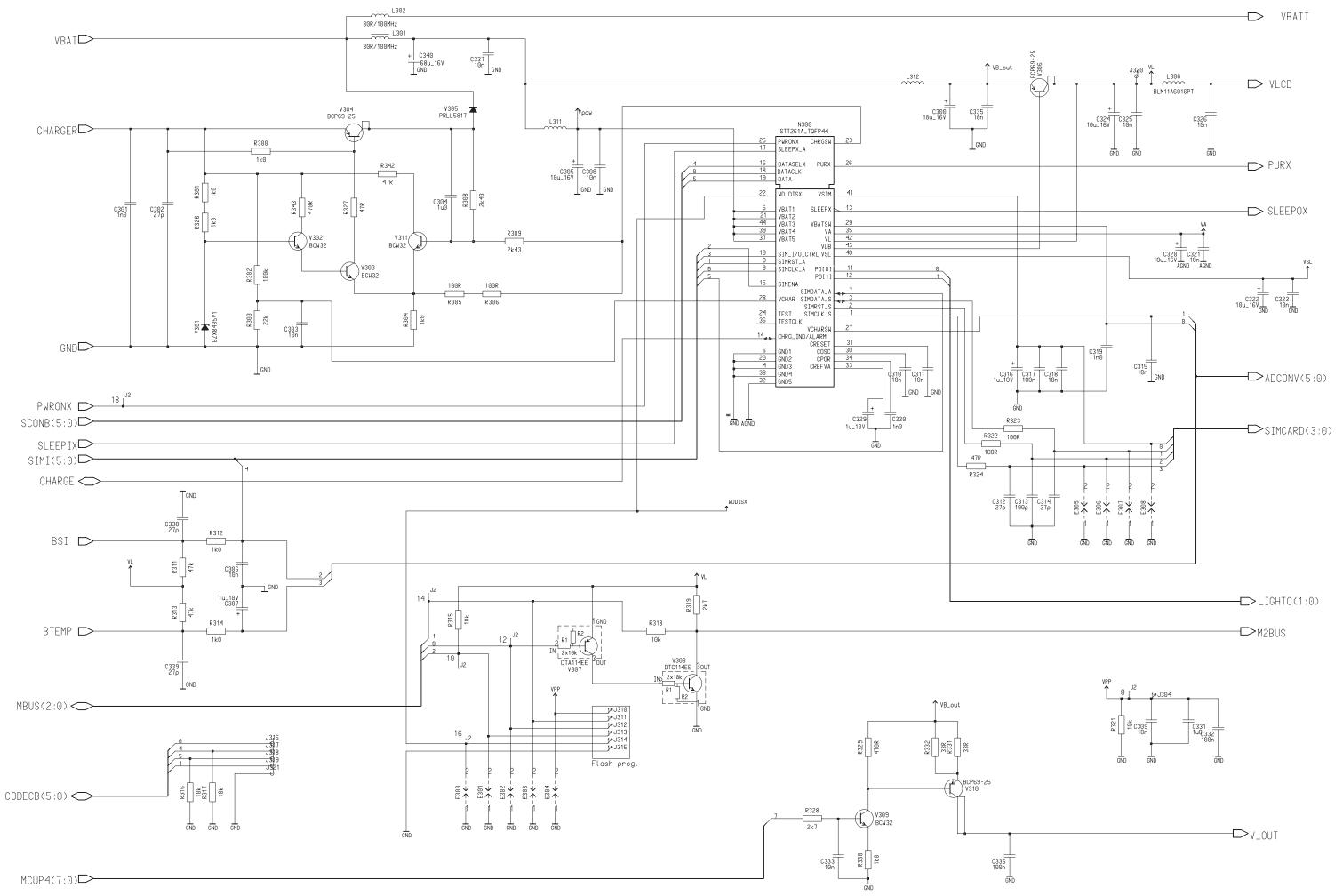
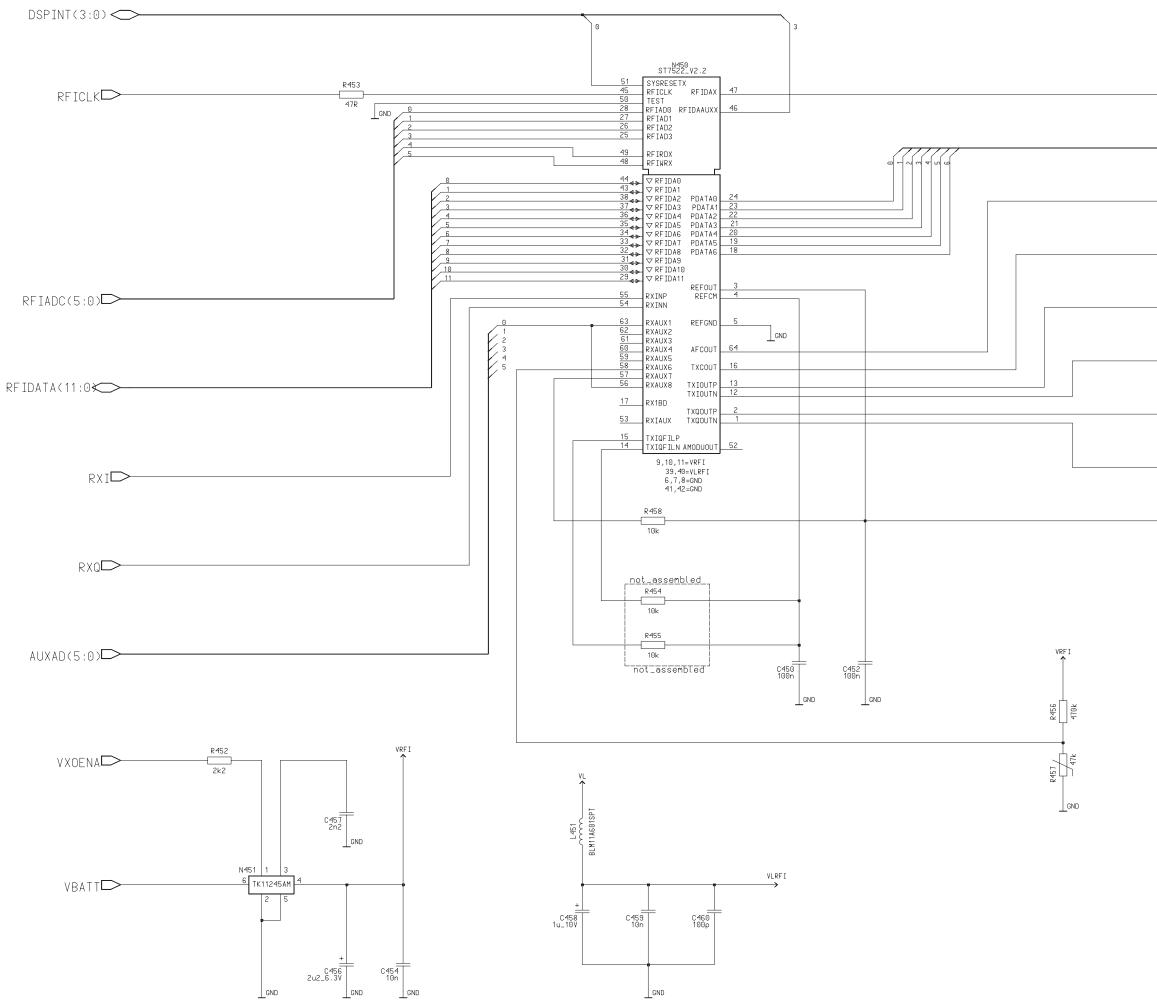


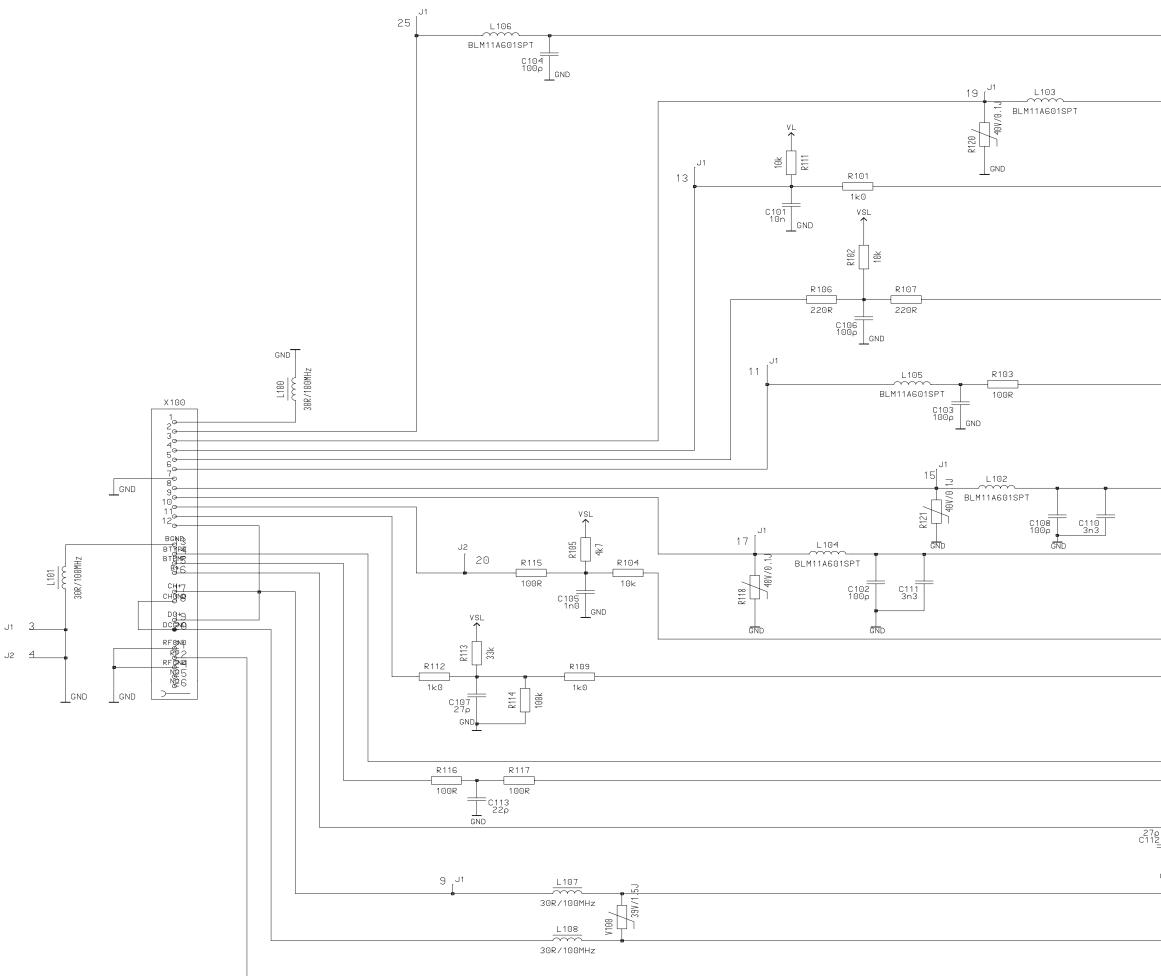
Figure 37 BB / RF Analog Interface



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——————————————————————————————————————
- RFIPORT(6:0)
-DTXC
-DTXIP
— DTXIN
-DTXQP
— DTXQN

Figure 38 System Connector Circuit Diagram



	V_OUT
	XMIC_ID
	EXT_RF
	——————————————————————————————————————
	MBUS
	SGND
	XEAR_MUTE
7 J ¹ 5 J ¹	BTYPE BTEMP
21 J1	VBAT
GND	CHARGER+
	GND